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Amendments to the Claims

- 1. (ORIGINAL) A TFT comprising a polycrystalline silicon channel extending between a source and drain, a gate overlying the channel, and of a thickness to define an upstanding gate side wall, an LDD region, and a spacer overlying the LDD region, wherein the spacer comprises a conductive region that both overlies the LDD region and extends along the upstanding gate side wall.
- 2. (ORIGINAL) A TFT according to claim 1 wherein the conductive region comprises a layer that is thinner than the thickness of the gate and has a first portion overlying the LDD region and a second portion extending along the upstanding side wall of the gate.
- 3. (ORIGINLA) A TFT according to claim 2 wherein the conductive region comprises a layer of conductive material.
- 4. (ORIGINLA) A TFT according to claim 3 wherein the layer is a metallic layer deposited by sputtering.
- (ORIGINAL) A TFT according to claim 3 wherein the layer comprises a doped semiconductor material.
- 6. (CURRENTLY AMENDED) A TFT according to any one of claims 2 to 5claim 2 including a fillet over the first portion of the conductive region.
- 7. (ORIGINAL) A method of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:
- (a) providing a gate separated from a polycrystalline silicon layer by an insulating layer;
- (b) implanting a dopant into the polycrystalline silicon layer using the gate as a mask;

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- (c) forming a spacer after step (b) adjacent to the gate that comprises a conductive region which overlies the polycrystalline silicon layer and extends along the gate side wall; and
- (d) implanting a dopant into the polycrystalline silicon layer using the gate and the spacer as a mask to form a source or drain region, such that the spacer overlies an LDD region in the polycrystalline silicon layer between the source or drain region and the channel.
- 8.. (ORIGINAL) A method according to claim 7 wherein step (c) comprises depositing a layer of conductive material over the polycrystalline silicon layer and the gate, and selectively etching the deposited layer of conductive material to form the spacer with a first portion overlying the polycrystalline silicon layer and a second portion extending along on the side wall of the gate.
- 9. (ORIGINAL) A method according to claim 9 including depositing the layer of conductive material to a thickness which is less than that of the gate.
- 10. (CURRENTLY AMENDED) A method according to claim 8 or 9 including depositing the conductive material in a non-conformal layer.
- 11. (CURRENTLY AMENDED) A method according to any one of claims 8 to 10 claim 8 including depositing the layer by sputtering.
- 12. (CURRENTLY AMENDED) A method according to any one of claims 8 to 11 claim 8 including depositing said layer as a metallic layer.
- 13. (CURRENTLY AMENDED) A method according elaim 8 or 9to claim 8 wherein the selective etching of the conductive layer is carried out by forming a fillet over the first portion thereof, and selectively etching the layer where not protected by the fillet.

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- 14. (ORIGINAL) A method according to claim 11 including depositing a further layer on said conductive layer, and selectively etching the further layer to form the fillet therefrom.
- 15. (ORIGINAL) A method according to claim 14 including depositing the further layer as a conformal layer.
- 16. (ORIGINAL) A method according to claim 14 including depositing the further layer as a Si containing layer.
- 17. (CURRENTLY AMENDED) A method according to any one of claims 13 to 16-claim 13 including depositing the further layer by CVD,
- 18. (ORIGINAL) A TFT substantially as hereinbefore described with reference to the accompanying drawings
- 19. (ORIGINAL) A method of fabricating a TFT substantially as hereinbefore described with reference to the accompanying drawings.